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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
MOON, SEOKYUN	
ART UNIT	**PAPER NUMBER**
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,779	KENNEDY ET AL.	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 11-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-13* is/are allowed.

6)☒ Claim(s) *1 and 14-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The Applicants' arguments regarding 35 U.S.C. 112, sixth paragraph filed on May 23, 2007 have been fully considered but they are not persuasive.

The Applicants pointed out, "*Simmonds does not disclose, teach, or suggest the structural or functional elements, or the equivalents thereof, corresponding to the structure, material or acts described in the specification (as per 35 U.S.C. 112 six paragraph) of the synchronization means of the present invention*" [page 11 lines 10-13].

Examiner respectfully disagrees.

According to the MPEP Section 2181, there are three conditions for invoking 35 U.S.C. 112, six paragraph. The three conditions are:

1) the claim limitations must use the phrase "means for" or "step for;"

2) the "means for" or "step for" must be modified by functional language; and

3) the phrase "means for" or "step for" must not be modified by sufficient structure, material, or acts for achieving the specified function.

In the current Application, claim 1 discloses, "*means for synchronizing... comprising: a master sync signal generator...; a signal generating means for receiving...; a comparison means for determining...*". In this claim, "*means for synchronizing*" is modified by "*master sync signal generator*", "*signal generating means*", and "*comparison means*".

Therefore, it is not proper to invoke 35 U.S.C. 112, six paragraph for the claim limitation, "*means for synchronizing*".

2. The Applicants' arguments regarding the combination under 35 U.S.C. 103(a) are moot in view of the new ground of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1, 14, 19-26** are rejected under 35 U.S.C. 102(b) as being anticipated by Hwang (US 6,337,682).

As to **claim 1**, Hwang teaches an image display system for synchronizing the display of images on a plurality of display devices (the display panel of "*the flat panel display apparatus*" and the display of the "*personal computer system*") [col. 1 lines 21-23], comprising:

a first computer system ("*personal computer system*") [col. 1 lines 21-23] generating a first signal ("*analog video signal*") representing first image data to be displayed on a first display device;

a second computer system ("*the flat panel display apparatus*") [col. 1 lines 21-25] generating a second signal ("*digital video signal*") representing second image data to be displayed on a second display device; and

means for synchronizing the first and second image data [fig. 3], the synchronizing means comprising:

a master sync signal generator generating a master sync signal ("*Hsync*"), and

a signal generating means (a combination of "*micro-controller 60*" and "*PLL 40*") for receiving the master sync signal and generating a video clock signal ("*CLK 1*") from the master sync signal wherein the video clock signal is synchronized with the master sync signal;

a comparison means (a combination of "*phase detector 70*" and "*comparator 65*") for determining if the video clock signal is no longer synchronized with the master sync signal [col. 5 lines 41-44];

wherein in response to the comparison means determining that the video clock signal is no longer synchronized with the master sync signal, the signal generating means reestablishes the synchronization between the video clock signal and the master sync signal [col. 6 lines 27-38]; and

wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a convergence time, wherein the duration of the convergence time is programmable (by adjusting the frequency divisional value, the frequency of the sampling clock signal CLK1 is adjusted).

As to **claim 14**, Hwang teaches that the signal generating means comprises a video input/output module comprised of a phase locked loop circuit ("*PLL 40*") and a programmable digital rate controller ("*Micro-controller 60*");

wherein the phase-locked loop circuit ("*PLL 40*") generates the video clock signal ("*CLK 1*");

wherein the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal [col. 6 lines 27-38];

wherein the programmable digital rate controller determines if the video clock signal is no longer synchronized with the master sync signal [col. 5 lines 41-44]; and

wherein the programmable digital rate controller further controls a lock responsiveness rate at which the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal (by adjusting the frequency divisional value, the frequency of the sampling clock signal CLK1 is adjusted), wherein a faster lock responsiveness rate results in a shorter convergence time and a slower lock responsiveness rate results in a longer convergence time (as the frequency divisional

value is adjusted, the lock responsiveness rate increases/decreases and thus results in that the locking occurs within a shorter / a longer time period).

As to **claim 19**, Hwang teaches the first and second image data comprising respective video images processed by a respective first video input/output module of the first computer system (the input/output of the "*personal computer system*") and a respective second video input/output module of the computer system ("*flat panel display apparatus*").

As to **claim 20**, Hwang [fig. 3] teaches the video input/output module comprising a video generator ("*ADC 20*") for generating a video signal in response to the video clock signal which is synchronized to the master sync signal.

As to **claim 21**, Hwang inherently teaches each of the first image data and the second image data comprising a respective computer graphic image since each of the display panel of Hwang's computer and the display panel of Hwang's flat panel display apparatus displays computer graphic images.

As to **claim 22**, Hwang inherently teaches each of the first and second computer systems further comprising a respective graphic processor for generating the respective computer graphics image since it is required for Hwang's computer and the flat panel display to include graphic processors to generate images on the display panels.

As to **claim 23**, Hwang teaches each graphics processor generating the computer graphics image in response to the video clock signal which is synchronized to the master sync signal [col. 5 line 65 – col. 6 line 2].

As to **claim 25**, Hwang teaches the image display system,

wherein the signal generating means comprises a video input/output module [fig. 3];

wherein the first computer system ("*personal computer system*") comprises the master sync signal ("*Hsync*") generator [col. 1 lines 21-25];

wherein the second computer system comprises the video input/output module [fig. 3]; and

wherein the video input/output module synchronizes to the master sync signal ("*Hsync*") received from the master sync signal generator;

wherein the first computer system is a master computer system and the second computer system is a slave display system [col. 1 lines 21-25].

As to **claim 26**, Hwang teaches the master sync signal being generated from a graphic processor of the master computer system [col. 1 lines 21-25].

As to **claim 24**, Hwang teaches the signal generating means comprising a video input/output module, the first computer system comprising a video input/output module, and the second computer system comprising a video input/output modules which receives master sync signal from the master sync signal generator, as discussed with respect to the rejection of claim 25.

Hwang does not expressly disclose the master sync signal generator being external to the first computer system and the video input/output module of the first computer to receive the master sync signal.

However, as Examiner acknowledges that specifying the master sync signal generator being external to the first computer system and the video input/output module of the first computer system receiving the master sync signal from the master sync signal generator, is not a required design layout/specification but is one of a plurality of design layouts, which includes a design layout described in claim 25, it is an obvious matter of design choice to have such an arrangement of the computer systems and to specify the master sync signal generator being external to the first and the second computer systems.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the image display system of Hwang to specify the master sync signal generator being external to the first and the second computer system since any one of the design layouts/options, i.e. including the master sync signal generator in the first computer system or placing the master sync signal

generator external to the first and the second computer systems would perform equally well at synchronizing the video clock signal outputted from the second computer system to the master sync signal.

Allowable Subject Matter

5. **Claims 15-18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. **Claims 11-13** are allowed.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (572) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 3, 2007

- s.m.

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER